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EXAMINER	
JELINEK, BRIAN J	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,007	SUZUKI, NOBUO	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *3/1/2005 (amendment)*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 3/1/2005 of application no. 09/824,007 filed on 4/3/2001 in which claims 1-19 are currently pending.

Drawings

The objection to the drawings is withdrawn in view of the Applicant's arguments.

Claim Objections

Claim 1 is objected to because of the following informalities: there is insufficient antecedent basis for the limitation in the claim.

Claim 1 recites the limitation "said reset signal lines" in the last line of the claim.

Claim 1 further recites "a reset signal line disposed for each pixel row" and "each said reset signal line receiving a reset signal"; it is not clear which one of the reset signals is the "said reset signal" or if the reset signal resets all of the rows at the same time.

Arguments

The Applicant's arguments have been fully considered but they are not persuasive. Please refer to the following office action, which clearly sets forth the reasons for non-persuasiveness.

The Applicant asserts that Roberts fails to disclose "an overall reset controller positioned within a column-directional shifter for supplying the reset signal to said reset signal lines at one time" and "the overall reset controller supplies a rest signal to said reset signal lines at one time".

In response, the Examiner briefly summarizes the cited description of the control cache (Fig. 1, element 208). Roberts discloses that the control cache performs memory functions so that pixel addresses, commands for pixel resetting, and taking a "snap shot" of a particular window or the entire array can be fed into the imaging device 10 using a smaller number of connecter pads. Furthermore, Roberts discloses a decoder and latch circuit (Fig. 1, element 24; Fig. 4) that is connected to the control cache and receives row addresses, which the decoder circuit decodes in order to select pixels for resetting. In particular, ADDRST is decoded into row reset 112 and produces the output signal 124, which is applied to address trace 58 (Fig. 2) to select a row of pixels for resetting. As a result, it is clear that the decoder and latch circuit (Fig. 1, element 24; Fig. 4) is a reset controller positioned within a column-directional shifter for supplying the reset signal to the reset signal lines. For further clarification, it appears to the Examiner that the control cache 208 and decoder circuit 24 of Roberts are substantially equivalent to the Applicant's controller (Fig. 1A, element 60) and reset row shifter (Fig. 1A, element 45), respectively.

Furthermore, in response to the Applicant's argument that Roberts does not disclose "the overall reset controller supplies a rest signal to reset signal lines at one time", the Examiner notes that Roberts discloses an alternate embodiment comprising

an additional transistor (Fig. 9, element 200) in order to simultaneously reset all of the pixels in the array (Fig. 12, element 28-50). Please note that the features of Fig. 9 are analogous in structure or function to features described in Fig. 2 and are referenced with the same numbers used previously (col. 11, lines 50-67), with the addition of transistor (Fig. 9, 200). Furthermore, the cited passage, col. 13, lines 30-34, discloses the "snap shot" mode of Fig. 9. Roberts explicitly discloses the snap shot capability "allows the pixels of the array to all be simultaneously reset" as a result of the additional functionality provided by transistor 200 (col. 12, lines 28-50). Consequently, it is clear that Roberts discloses that the overall reset controller supplies a rest signal to the reset signal lines at one time.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Roberts (U.S. Pat. No. 5,452,004).

Please note that the features of Fig. 9 are analogous in structure or function to features described in Fig. 2 (col. 11, lines 50-67), with the addition of transistor (Fig. 9, 200).

Regarding claim 1, Roberts discloses a MOS-type solid-state image pickup device, comprising: a semiconductor substrate (Fig. 1, element 14); a large number of pixels arranged in one surface of the semiconductor substrate in an array having a plurality of rows and a plurality of columns (Fig. 1, element 12), each pixel (Fig. 1, element 40) includes (a) a photoelectric converter element (Fig. 9, element 42) and (b) a switching circuit (Fig. 9, element 40) electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge (col. 8, line 44-55); a row selection signal line (Fig. 4, element 114; Fig. 9, element 48) disposed for each pixel row and being electrically connected to associated switching circuits, each row selection signal line receiving a row selection signal for controlling the generation of the output signal; a plurality of output signal lines (Fig. 9, CCVL; Fig. 1, element 28) each of which being associated with at least one pixel column and receiving the output signal from associated switching circuits; a reset signal line (Fig. 4, element 112; Fig. 1, element 28) disposed for each pixel row and being electrically connected to associated switching circuits, each reset signal line receiving a reset signal for controlling the discharge of the electric charge (col. 8, lines 44-55; col. 7, lines 11-26); and an overall reset controller (Fig. 1, element 208; Fig. 9, element 200; col. 12, lines 28-50) for supplying the reset signal to the reset signal lines at a time.

Regarding claim 2, Roberts discloses each switching circuit comprises: an output (amplifying) transistor (Fig. 9, element 74) including a control terminal electrically connected to the photoelectric converter element for generating the output signal; a row

selection transistor (Fig. 9, element 46) electrically connected in series to the output transistor, the row selection transistor including a control terminal electrically connected to the row selection signal line; and a reset transistor (Fig. 9, element 70) electrically connected to the photoelectric converter element, the reset transistor including a control terminal electrically connected to the reset signal line.

Regarding claim 3, Roberts teaches a plurality of constant-voltage supply lines (Fig. 9, element 54) extending in a direction of the pixel rows for receiving a constant voltage, each pixel row being associated with one of the constant-voltage supply lines, each constant-voltage supply line being electrically connected to the output transistors and the reset transistors in the associated pixel column or row.

Regarding claim 4, Roberts teaches a readout row-shifter (Fig. 4, element 102) for sequentially supplying the row selection signal to the row selection signal lines; a reset row-shifter (Fig. 4, element 100) for sequentially supplying the reset signal to the reset signal lines; and an image signal outputting device electrically connected to the output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal (col. 9, lines 1-7).

Regarding claim 5, Roberts teaches an analog signal generator for converting the output signal generated on each output signal line (Fig. 9, CCVL) into an analog voltage signal (Fig. 6, Vout; col. 9, lines 1-17); and a row-directional shifter for controlling operation of the analog signal generator and for being sequentially outputted the analog voltage signal from the analog signal generator (col. 1, lines 15-20 and 62-65).

Regarding claim 6, Roberts teaches an analog signal generator for converting the output signal generated on each output signal line into an analog voltage signal (col. 9, lines 1-17); and an analog-to-digital converter (Fig. 6, element 166) for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom because a buffer is inherent in an A/D converter since the result is latched and held for a time in order to provide an output value.

Regarding claim 7, Roberts teaches a controller (Fig. 1, element 208) for controlling operations (col. 13, lines 22-44) of the overall reset controller, the readout row-shifter, the reset row-shifter, and the image signal outputting device.

Regarding claim 8, Roberts teaches a transfer signal line (Fig. 9, element 48) disposed for each pixel row and being electrically connected to associated switching circuits; and a transfer control row-shifter for sequentially supplying (col. 5, line 6-13; col. 1, lines 62-65) a transfer control signal controlling the generation or the discharge of the output signal to the transfer signal lines, and each switching circuit further comprises a charge transfer transistor (Fig. 9, element 46) electrically connected to the photoelectric converter element, the output transistor, and the reset transistor, the charge transfer transistor including a control terminal electrically connected to the transfer signal line.

Regarding claim 9, Roberts teaches a plurality of constant-voltage supply lines (Fig. 9, Vssa) extending in a direction of the pixel column or row for receiving a constant

voltage, each pixel column or row being associated with one of the constant-voltage supply lines, each constant-voltage supply line being electrically connected to the output transistors, the reset transistors and the charge transfer transistor in the associated pixel column or row.

Regarding claim 10, please see the 102 rejection of claim 4. Roberts further discloses a transfer control row-shifter for sequentially supplying the transfer control signal to the transfer signal lines (Fig. 1, element 208).

Regarding claim 11, please see the 102 rejection of claim 5.

Regarding claim 12, please see the 102 rejection of claim 6.

Regarding claim 13, please see the 102 rejection of claim 7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004) in view of Ernest et al. (U.S. Pat. No. 4, 827,348).

Regarding claim 14, please see the 102 rejections of claims 1 and 4 and note that Roberts teaches a digital camera, comprising: a MOS-type solid-state image pickup device, comprising: (i) a semiconductor substrate; (ii) a large number of pixels arranged

in one surface of the semiconductor substrate in an array having a plurality of rows and a plurality of columns, each pixel includes (a) a photoelectric converter element and (b) a switching circuit electrically connected to the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in the photoelectric converter element and discharge of the electric charge; (iii) a row selection signal line disposed for each pixel row and being electrically connected to associated switching circuits, each row selection signal line receiving a row selection signal for controlling the generation of the output signal; (iv) a plurality of output signal lines each of which being associated with at least one pixel column and receiving the output signal from associated switching circuits; (v) a reset signal line disposed for each pixel row and being electrically connected to associated switching circuits, each reset signal line receiving a reset signal for controlling the discharge of the electric charge; (vi) a readout row-shifter for sequentially supplying the row selection signal to the row selection signal lines; (vii) a reset row-shifter for sequentially supplying the reset signal to the reset signal lines; (viii) an overall reset controller for supplying the reset signal to the reset signal lines at a time; and (ix) an image signal outputting device electrically connected to the output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal; and an image signal processor for generating mobile picture data or still picture data using the image signal outputted from the MOS-type solid-state image pickup device; and a mobile picture mode controller (Fig. 1, element 208) electrically connected to the MOS-type solid-state image pickup device for continually control operation thereof for repeatedly conducting

(a) an image readout operation in which the row selection signal is sequentially supplied from the readout row-shifter to a predetermined number of row selection signal lines for sequentially outputting from the image signal outputting device an image signal representing the output signal generated on each the output signal line and (b) an electronic shutter operation in which the reset signal is sequentially supplied from the reset row-shifter to the reset signal supply lines at least associated with the pixel row as an object of the image signal readout operation for sequentially discharge electric charge accumulated in the photoelectric converter elements.

Furthermore, Roberts teaches the use of an additional transistor (Fig. 9, element 200) in an alternative embodiment that enables a global reset and "snap shot" capability (col. 12, lines 28-38). One of ordinary skill in the art would have provided the additional transistor of Roberts alternative embodiment for the purpose of enabling still capture in addition to motion video capture. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the additional transistor of Roberts alternative embodiment for the purpose of enabling still capture in addition to motion video capture. Further still, Roberts teaches a still picture indication signal generator for generating a still picture indication signal indicating shooting of a still picture (col. 12, lines 28-38) because it a still picture indication signal is inherent in taking a snapshot.

Although Roberts teaches the use of an electronic shutter (col. 12, lines 46-50), Roberts does not disclose a light shielding device capable of interrupting light incident to the image pickup device for a predetermined period of time after an overall reset

operation. However, Ernest et al. teaches a mechanical shutter for interrupting light incident to an image pickup device (Fig. 3, element 24; col. 4, lines 11-15), which remains closed for a predetermined period of time until the still image is read out following an overall reset (Fig. 2). One of ordinary skill in the art would have provided the mechanical shutter of Ernest et al. for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode (col. 3, lines 7-13). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the mechanical shutter of Ernest et al. for exposure control in a dual mode camera in order to permit high shutter speed in the still mode and electronic shuttering in the video mode.

Regarding claim 15, Ernest et al. teaches when in the video mode (corresponding to an electronic shutter operation), and the still picture indication signal is outputted, the still picture mode controller does not interrupt the operation (Figs. 1 and 2); when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, the still picture mode controller conducts once the image signal readout operation after the electronic shutter operation (Figs. 1 and 2); and then the first still picture mode controller conducts the overall reset operation (col. 6, lines 28-59) when a global reset is operated in preparation for a second still picture.

Regarding claim 16, please see the 102 rejection of claim 8 and note that Roberts teaches a transfer signal line disposed for each pixel row and being electrically connected to associated switching circuits; and a transfer control row-shifter for

sequentially supplying a transfer control signal controlling the generation or the discharge of the output signal to the transfer signal lines, and each the switching circuit further comprises a charge transfer transistor electrically connected to the photoelectric converter element, the output transistor, and the reset transistor, the charge transfer transistor including a control terminal electrically connected to the transfer signal line.

Furthermore, Roberts teaches a mobile picture mode controller (Fig. 1, element 208) or the first still picture mode controller conducting the transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each transfer signal lines associated with the pixel row as an object of the operation.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roberts (U.S. Pat. No. 5,452,004), in view of Ernest et al. (U.S. Pat. No. 4, 827, 348), and further in view of Soeda et al. (U.S. Pat. No. 5,382,974).

Regarding claim 17, Roberts teaches motion video and still image capture (col. 1, line 55-col. 2, line 5; col. 12, lines 28-38). Furthermore, Ernest et al. teaches a shutter that interrupts light for a predetermined period of time (please see the 103 rejection of claim 14). Neither Roberts nor Ernest et al. teaches the use of a strobe device or a controller for a second still picture mode comprising a strobe device.

However, Soeda et al. teaches a strobe device (Fig. 1, element 20) for emitting flash light when a predetermined signal is received (Fig. 5) or the strobe device installing device for installing therein; a second still picture mode controller (strobe

mode: col. 13, lines 27-31; Fig. 3, elements S8 and S18) electrically connected to the image pickup device for controlling in place of a mobile mode controller, when the still picture indication signal is outputted; a strobe device operation signal is generated for operating the strobe device (Fig. 5); a shutter is operated for a predetermined period of time after strobe device operation signal is generated (Fig. 5); and a still picture mode specifying device (Fig. 3, element S8; col. 14, lines 24-38) for beforehand specifying a still picture mode controller to be operate when the still picture indication signal is outputted.

One of ordinary skill in the art would have provided the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3). As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the strobe of Soeda et al. with the imager of Roberts and Ernest et al. for the purpose of increasing the maximum photographable distance to an object and to obtain a high quality image (col. 13, line 65-col. 14, line 3).

Regarding claim 18, Roberts teaches motion video and still image capture (col. 1, line 55-col. 2, line 5; col. 12, lines 28-38). Roberts does not specifically teach that a still picture mode does not interrupt a video mode when a still picture mode is indicated. However, Ernest et al. teaches an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, a still picture mode controller does not interrupt the operation; and when an electronic shutter operation is being executed at a point of time when the still

picture indication signal is outputted, a still picture mode controller conducts once the image signal readout operation after the electronic shutter operation; and then a still picture mode controller conducts the overall reset operation (Fig. 2).

Regarding claim 19, please see the rejection for the 103 rejection of claim 16.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 8:00 am - 4:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Groody can be reached at (571) 272-7950. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
4/19/2005

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Art Unit ~~262~~ 2615